

FIG. 1 (PRIOR ART)

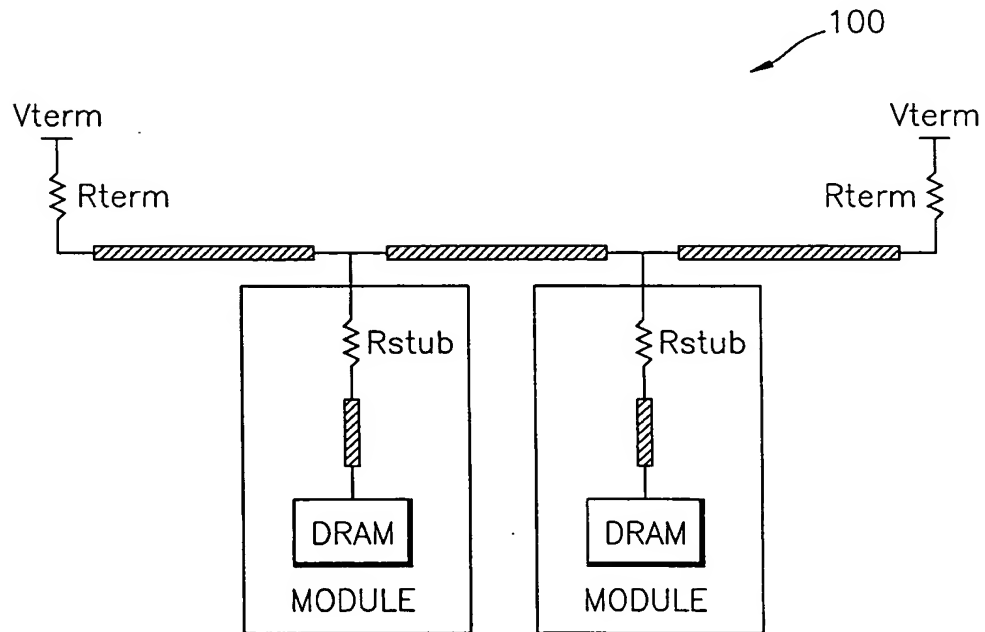
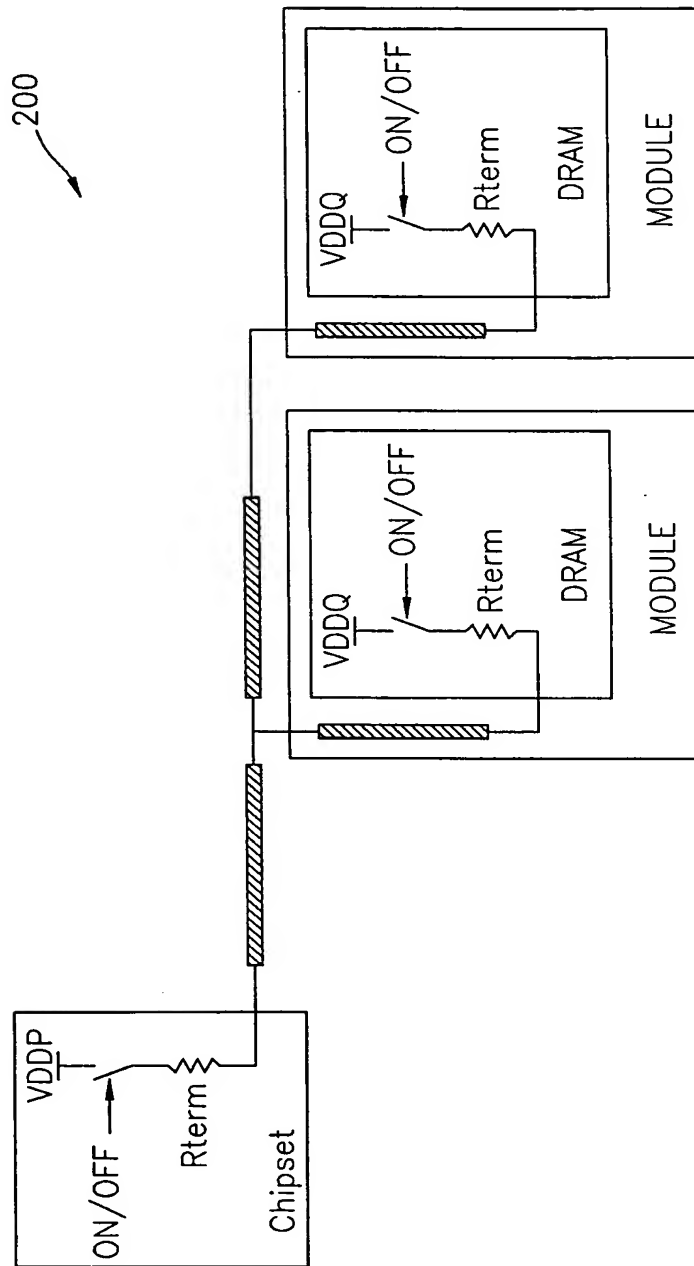


FIG. 2 (PRIOR ART)



DEVICES AND METHODS FOR CONTROLLING ACTIVE TERMINATION RESISTORS IN A
MEMORY SYSTEM

Application No. [NEW] - Attorney Docket No. SEC.924C

Inventor: Kye-Hyun KYUNG

FIG. 3

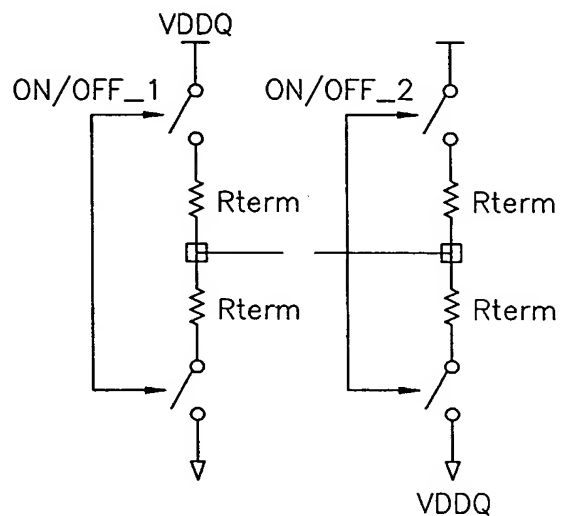


FIG. 4

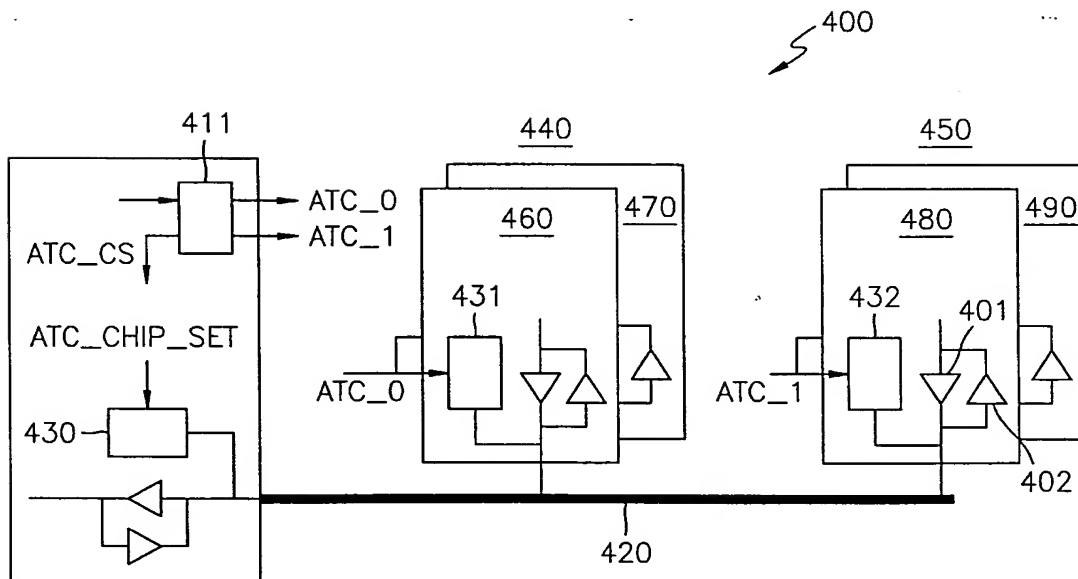


FIG. 5A

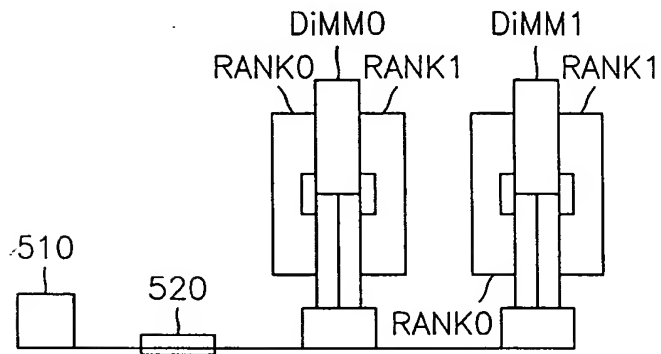
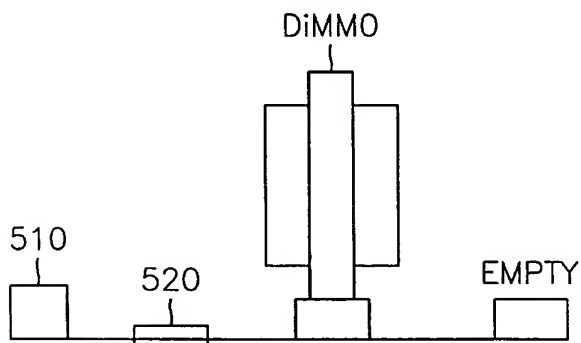


FIG. 5B



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FIG. 6

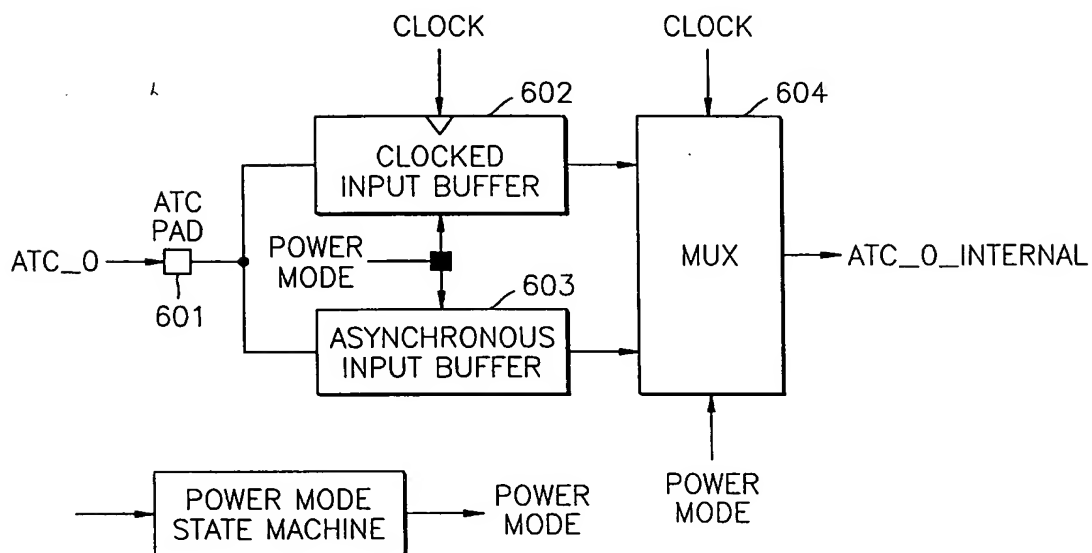


FIG. 7A

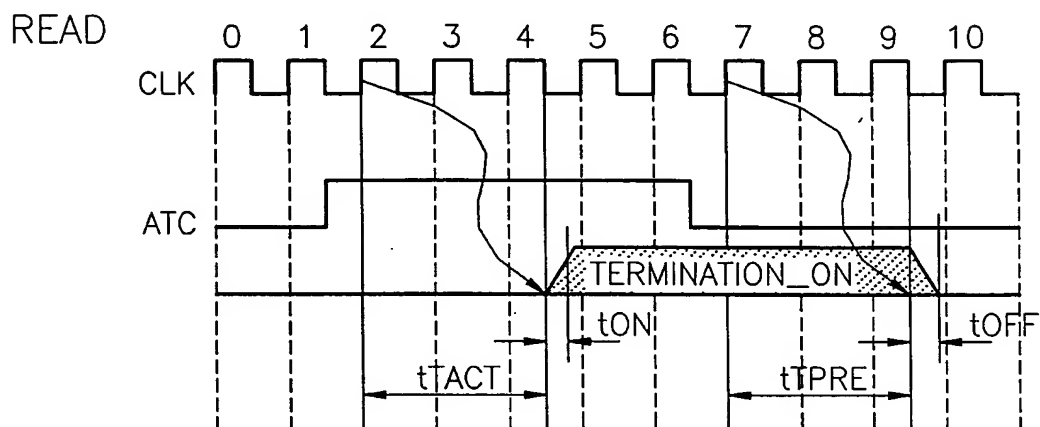
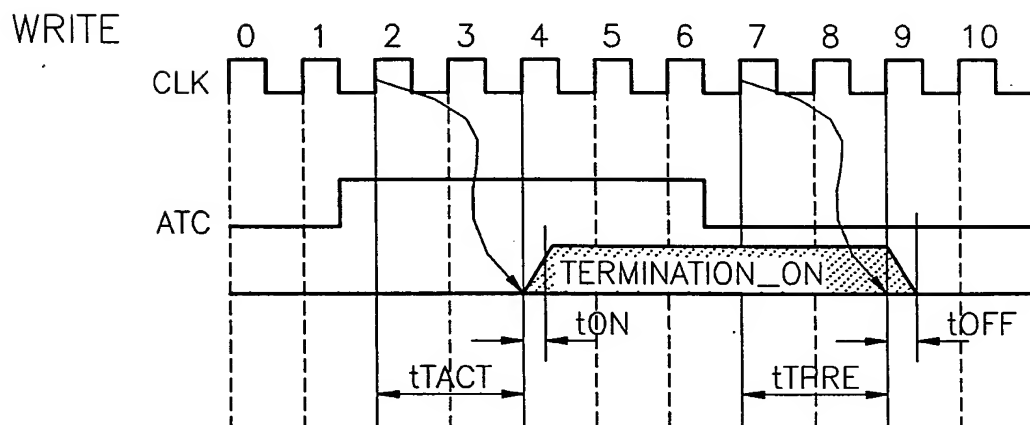


FIG. 7B



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FIG. 8

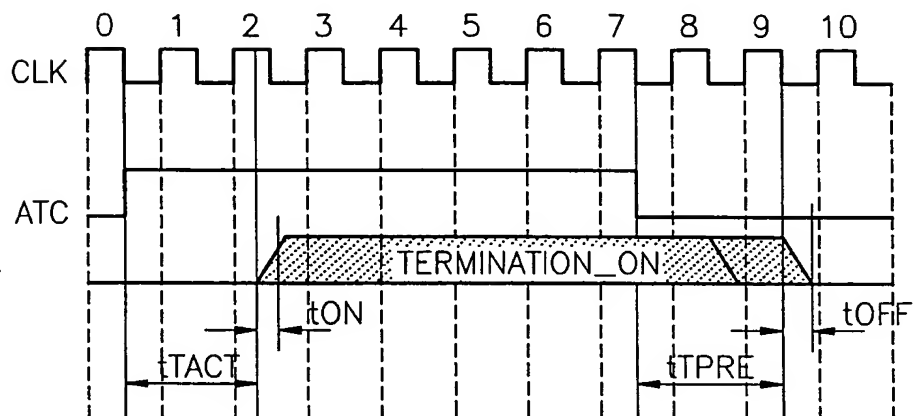


FIG. 9A

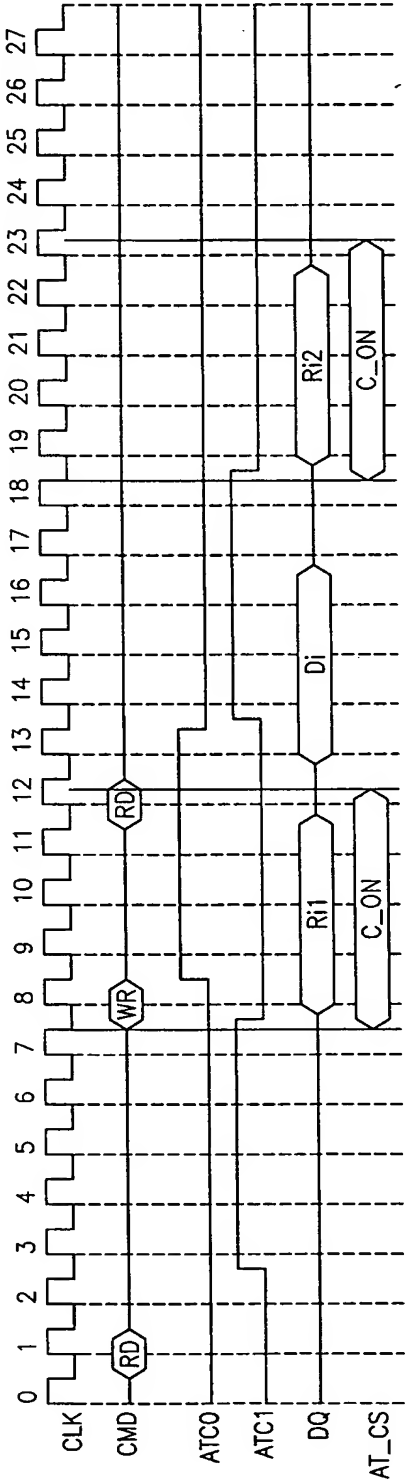
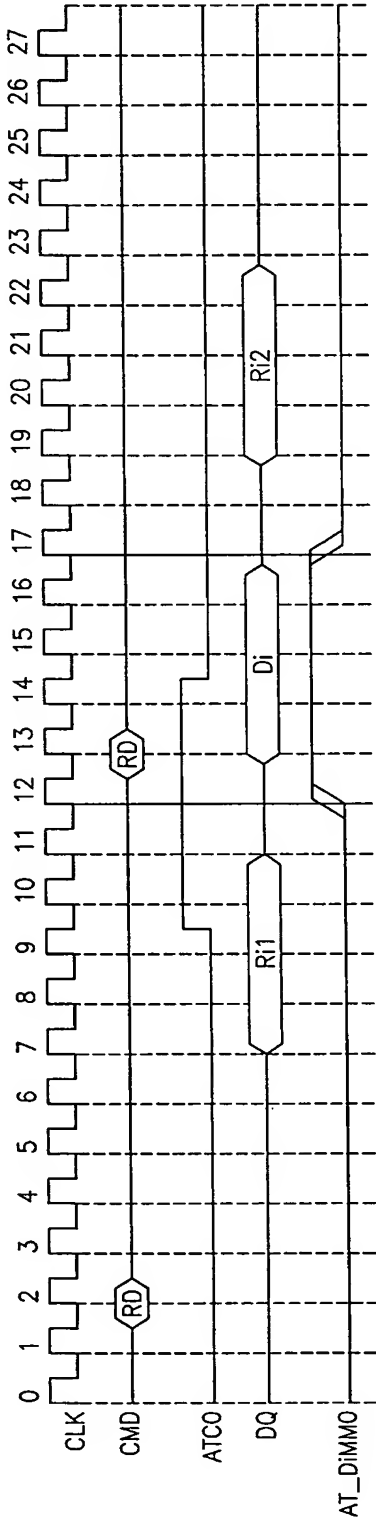


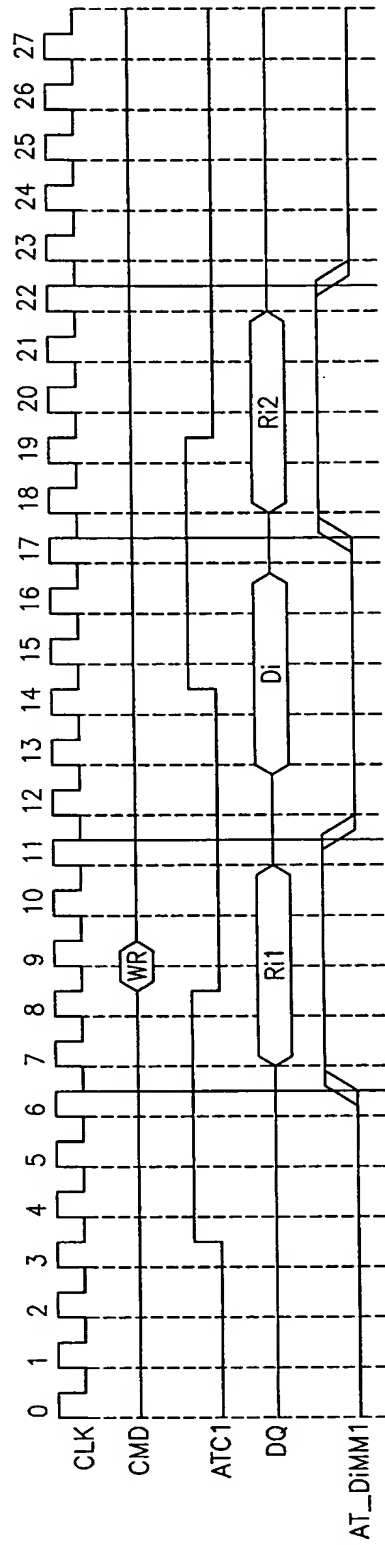
FIG. 9B



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FIG. 9C



The timing diagram shows the following sequence of events:

- CLK**: A periodic clock signal.
- CMD**: Command signal. It has three pulses labeled **RD** (Read) at clock cycles 1, 10, and 14.
- ATC0**: Address/Command 0 signal. It is active (low) from cycle 8 to 13.
- ATC1**: Address/Command 1 signal. It is active (low) from cycle 2 to 12.
- DQ**: Data bus signal. It shows data transfers for **R1** (Read 1) from cycle 8 to 11, **R2** (Read 2) from cycle 21 to 24, and **Di** (Data In) from cycle 15 to 19.
- AT_CS**: Address/Command Chip Select signal. It has two pulses labeled **C_ON** (Chip On) from cycle 7 to 11 and from cycle 21 to 25.

The timing diagram illustrates the relationship between the clock (CLK) and the data signals (CMD, ATC0, DQ, AT_DIMM0) over 27 clock cycles. The clock signal is a periodic square wave. The data signals are shown as horizontal lines, indicating that they are constant low signals. The diagram also shows three read operations (RD) on the CMD signal and three read operations (Ri1, Di, Ri2) on the DQ signal. The ATC0 and AT_DIMM0 signals are constant low signals.

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FIG. 10C

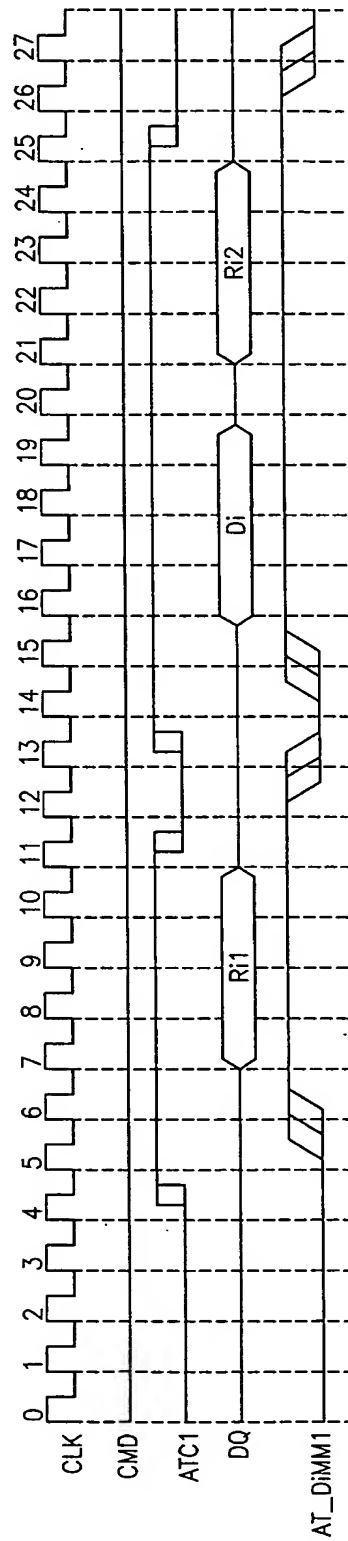


FIG. 11

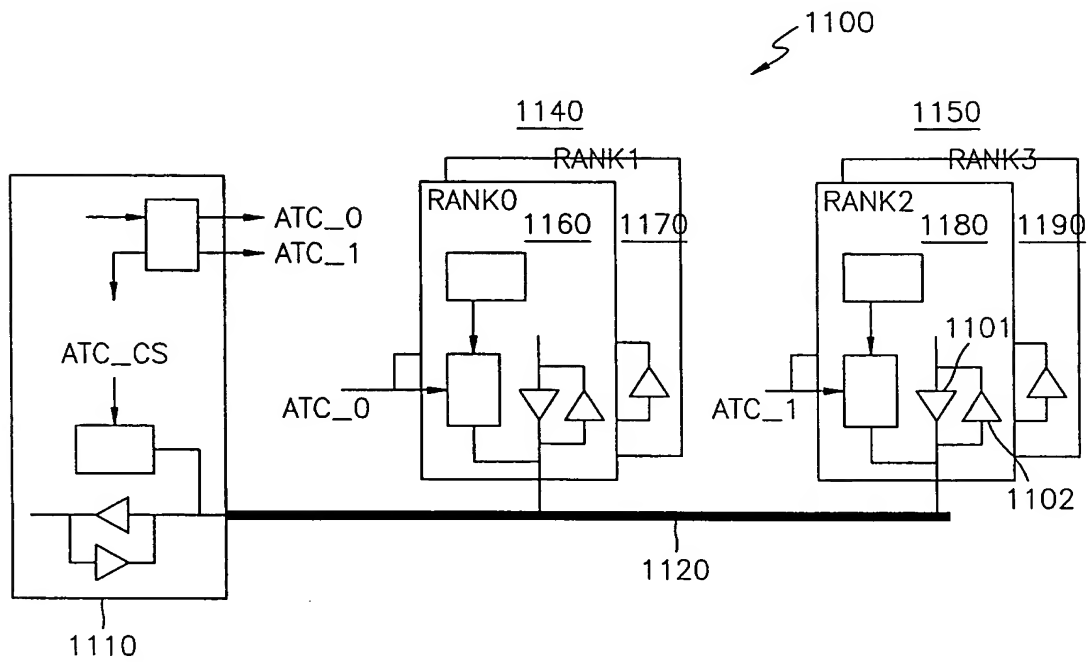


FIG. 12

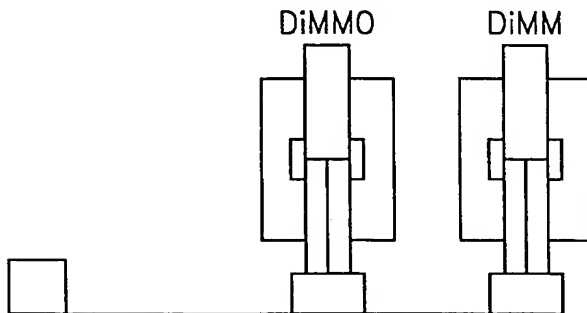


FIG. 13

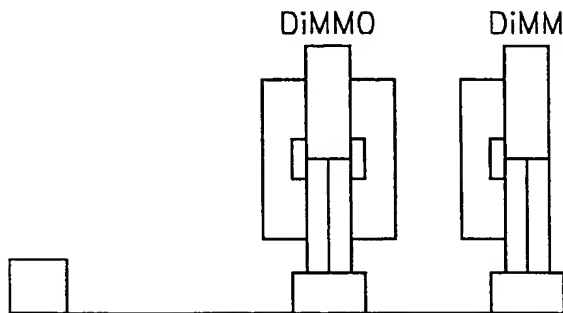


FIG. 14

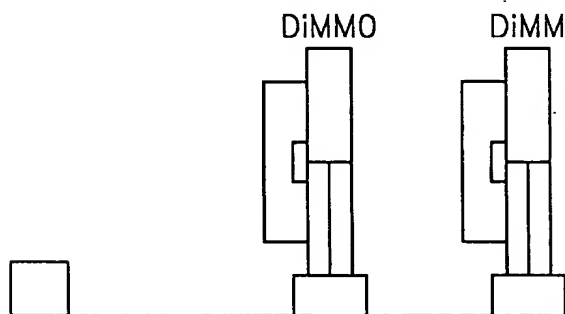


FIG. 15

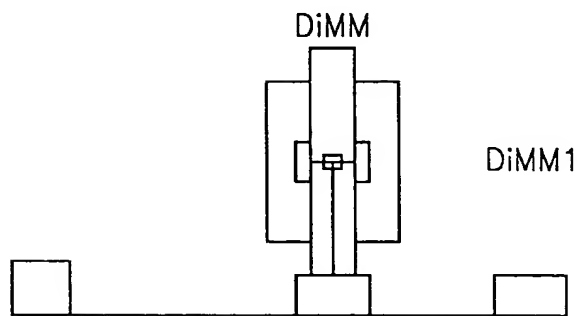


FIG. 16

